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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DEBJIT DAS SARMA

Appeal 2009-008047
Application 10/730,800
Technology Center 2100

Before JOSEPH F. RUGGIERO, ROBERT E. NAPPI, and CARLA M. KRIVAK, *Administrative Patent Judges*.

KRIVAK, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

Appellant appeals under 35 U.S.C. § 134(a) from a final rejection of claims 1-22. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellant's claimed invention is a method and apparatus for multiple pass extended precision floating point multiplication. The invention includes a floating point multiplier circuit with partial product generation logic configured to generate a plurality of partial products from multiplicand and multiplier values (Abstract).

Independent claims 10 and 16, reproduced below, are representative of the subject matter on appeal.

10. A method of operation of a multiplier circuit, comprising:

said multiplier circuit receiving an N-bit multiplicand value and an M-bit multiplier value;

said multiplier circuit generating a plurality of partial products from said multiplicand value and said multiplier value, wherein said plurality of partial products corresponds to a first portion of said multiplier value during a first partial product execution phase, and wherein said plurality of partial products further corresponds to a second portion of said multiplier value during a second partial product execution phase;

said multiplier circuit accumulating said plurality of partial products generated during said first partial product execution phase into a redundant product during a first carry save adder execution phase;

said multiplier circuit accumulating said plurality of partial products generated during said second partial product execution phase into said redundant product during a second carry save adder execution phase;

said multiplier circuit reducing a first portion of said redundant product to a multiplicative product during a first carry propagate adder phase; and

said multiplier circuit reducing a second portion of said redundant product to said multiplicative product during a second carry propagate adder phase;

wherein said first carry propagate adder phase begins after said second carry save adder execution phase completes.

16. A microprocessor comprising:

dispatch logic configured to issue multiply instructions to a floating-point unit; and

a floating-point unit coupled to said dispatch logic and configured to:

receive an N-bit multiplicand value and an M-bit multiplier value;

generate a plurality of partial products from said multiplicand value and said multiplier value, wherein said plurality of partial products corresponds to a first portion of said multiplier value during a first partial product execution phase, and wherein said plurality of partial products further corresponds to a second portion of said multiplier value during a second partial product execution phase;

accumulate said plurality of partial products generated during said first partial product execution phase into a redundant product during a first carry save adder execution phase;

accumulate said plurality of partial products generated during said second partial product execution phase into said redundant product during a second carry save adder execution phase;

reduce a first portion of said redundant product to a multiplicative product during a first carry propagate

adder phase; and reduce a second portion of said redundant product to said multiplicative product during a second carry propagate adder phase;

wherein said first carry propagate adder phase begins after said second carry save adder execution phase completes.

REJECTION and ANALYSIS

The Examiner rejected claims 1-22 under 35 U.S.C. § 101 as directed to non-statutory subject matter.

Appellant contends claims 1-9 are directed to an apparatus, claims 10-15 are directed to a method of operation of a multiplier circuit, and claims 16-22 are directed to a microprocessor having specific hardware elements (Reply Br. 3-5).

We agree with Appellant's arguments that claim 1 does more than recite algorithmic operations. That is, claim 1 recites with particularity the structure of an apparatus (Reply Br. 3). Thus, claim 1 and dependent claims 2-9 are directed to statutory subject matter.

With respect to claims 10-15, Appellant contends claim 10 "specifically limits the performance of those [method] actions to a particular type of apparatus; a multiplier circuit" (underlining omitted) (Reply Br. 4). However, the Examiner finds claim 10 encompasses any multiplier circuit and further, it covers the method of multiplying (Ans. 6).

We analyze the claims with respect to *Bilski v. Kappos*, 130 S. Ct. 3218, 3227 (2010). Under *Bilski*, the machine or transformation test is just one test for determining whether a claim is directed to non-statutory subject matter under § 101.

The U.S. Court of Appeals for the Federal Circuit explained the "machine-or-transformation test" for process claims as follows:

> The machine-or-transformation test is a two-branched inquiry; an applicant may show that a process claim satisfies § 101 either by showing that his claim is tied to a particular machine, or by showing that his claim transforms an article. *See* [*Gottschalk v.*] *Benson*, 409 U.S. [63], 70 [(CCPA 1972)]. Certain considerations are applicable to analysis under either branch. First, as illustrated by *Benson* and discussed below, the use of a specific machine or transformation of an article must impose meaningful limits on the claim's scope to impart patent-eligibility. *See Benson*, 409 U.S. at 71-72. Second, the involvement of the machine or transformation in the claimed process must not merely be insignificant extra-solution activity. *See* [*Parker v.*] *Flook*, 437 U.S. [584,] 590 [(1978)].

In re Bilski, 545 F.3d 943, 961-62 (Fed. Cir. 2008) (en banc).

Thus, the question before us is, if a machine is present as asserted by Appellant, is the machine's involvement extra-solution activity or field-of-use. That is, does this claim recite a practical application?

In the instant case, claim 10 recites a method of operation of a multiplier circuit. The only "machine" recited is the multiplier circuit that receives a multiplicand and a multiplier. The multiplier circuit generates a plurality of partial products, accumulates partial products into a redundant product during a carry save adder phase, reduces a first portion of the redundant product to a multiplicative product, wherein a first carry propagate adder phase begins after a second carry save adder phase. In view of the generic recitation of "multiplier circuit," we find there is no specific machine recited, as any device which performs these functions would reasonably be a "multiplier circuit." Further, the claim recites no extra-solution activity nor is their any practical application claimed for the

multiplication performed by the multiplier circuit recited in claim 10. Rather, the claim involves an algorithm in which a multiplicative product is generated; no practical application for that value is claimed. Also, claim 10 does not specify any particular type or nature of data, how or from where the data comes from, or what the data represents. Thus, claim 10 does not pass the machine or transformation test. Additionally, as in *Benson,* the claimed method encompasses all applications of the mathematical algorithm, as any device which could perform the steps is reasonably construed as a multiplier circuit. Therefore the "patent would wholly pre-empt the mathematical formula and in practical effect would be a patent on the algorithm itself." *Benson*, 409 U.S. at 72

With respect to claims 16-22, Appellant asserts claim 16 is directed to a microprocessor that includes dispatch logic and a floating point unit coupled to the dispatch logic, which are hardware elements (App. Br. 23). We agree with the Examiner that the "result produced by the invention is a mere mathematical result, which is a product of multiplying two number [sic]. The mathematical result clearly have [sic] no real world value because there is no practical application of the invention recited in the claim to make the result useful, concrete and tangible" (Ans. 6). Although Appellant asserts the effect of reducing costs in terms of die size and power consumption, the Examiner notes these features are not recited in the claims. Rather, the "result produced by the invention is the mathematical product of multiplying two numbers that is [sic] obtained from the first carry propagate adder phase and the second carry propagate adder phase." (Ans. 6)

The Federal Circuit has further recognized the Court's precedent in *Bilski* suggests "the 'mathematical algorithm' exception [an example of the

abstract idea judicial exception] applies to true apparatus claims." *In re Alappat*, 33 F.3d 1526, 1542 (Fed. Cir. 1994). Thus, the mathematical exception analysis used in "*Benson* . . . applies equally whether an invention is claimed as an apparatus or process, because the form of the claim is often an exercise in drafting." *Id.* (quoting *In re Johnson*, 589 F.2d 1070, 1077 (CCPA 1978) (internal quotation marks omitted)).

Therefore, we again apply the two prongs of the machine or transformation test. In doing so, claim 16 fails, as there is no limitation in the claim to a tangible practical application except multiplication. Claim 16 also encompasses substantially all practical applications of the mathematical algorithm (multiplication) as the claim is not limited to any field. Thus, as in *Benson,* the multiplication occurring has no practical application except in connection with a microprocessor, and therefore the "patent would wholly pre-empt the mathematical formula and in practical effect would be a patent on the algorithm itself." *Benson*, 409 U.S. at 72.

CONCLUSION

The Examiner erred in rejecting claims 1-9 under 35 U.S.C. § 101.

The Examiner did not err in rejecting claims 10-22 under 35 U.S.C. § 101.

DECISION

The Examiner's decision rejecting claims 1-9 is reversed.

The Examiner's decision rejecting claims 10-22 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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